



In the United States Patent and Trademark Office

Re the application of
Chakravarthy, et al. I-29660.1

Application No. 10/771,775 Art Unit: 2133

Filed: 2/2/2004 Examiner: Shelly A. Chase

Title: Using Pseudo-Pins in Generating Scan Test Vectors for Testing
an Embedded Core While Maintaining the IP Contained Therein

December 21, 2005

Asst. Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that the above correspondence is
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First Class Mail in an envelope addressed to:
Assistant Commissioner for Patents, P.O. Box 1450
Alexandria, VA 22313-1450 on December 21, 2005.

Lawrence J. Bassuk, Reg. No. 29,043

Dear Sir:

Transmitted herewith is an amendment in this application.

The fee has been calculated as shown below.

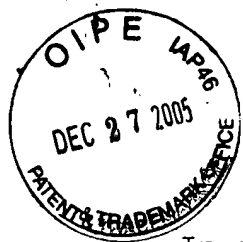
CLAIMS AS AMENDED						
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE	ADDITIONAL FEE
Total Claims	2	Minus	20	= 0	x \$50 =	\$ 0
Ind. Claims	1	Minus	3	= 0	x \$200 =	\$ 0
TOTAL ADDITIONAL FEE FOR THIS AMOUNT						\$ 0

Under 37 C.F.R. § 1.16(k) please charge the total additional fee, and
any further fees, or credit overpayment to Deposit Account No. 20-0668,
of Texas Instruments Incorporated.

Respectfully submitted,

Texas Instruments Incorporated
P.O. Box 655474, M/S 3999
Dallas, Texas 75265
(972) 917-4418

Lawrence J. Bassuk
Reg. No. 29,043
Attorney for Applicant



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for Testing an Embedded Core While Maintaining
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Amendment B Under 37 CFR 1.111

December 21, 2005

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Lawrence J. Bassuk
Lawrence J. Bassuk, Reg. No. 29,043

Responsive to the Examiner's Action of 05/31/2005, please
amend this application as follows:

In the Title:

Amend the title as follows:

~~Using pseudo-pins in generating scan test vectors for testing an embedded core while maintaining the IP contained therein~~ Generating an abbreviated netlist including pseudo-pin inputs and output nodes